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Patent
Attorney's Docket No. 032481-034

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)	
	)	
Mukesh K. PATEL, et al.	)	Examiner: [prior application: C. Das]
	)	
Application No.: to be assigned	)	
	)	Group Art Unit: [prior application: 2122]
Filed: concurrently herewith	)	
	)	
For: JAVA VIRTUAL MACHINE HARDWARE FOR RISC AND CISC PROCESSORS	)	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the application wherein a request for continuation application is concurrently filed, please amend the application as follows:

In the Claims:

Please cancel claims 1-36.

Please add new claims 37-237 as follows.

37. A system comprising:

a central processing unit having a register file, the central processing unit adapted to execute register-based instructions; and

a hardware unit associated with the central processing unit, the hardware unit adapted to convert Java bytecode instructions into register-based instructions, wherein the hardware unit is adapted to store at least one Java variable in the central processing unit's register file at a location separate from any operand stack, wherein at least one of the register-based instructions reference a register in the central processing unit's register file containing one of the at least one Java variable.

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